This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently amended)A semiconductor [[chip]]device having low metallization series resistance, the semiconductor device comprising:

~~a semiconductor substrate;~~

a metallization structure formed on [[said]]a semiconductor substrate;

an under bump metallurgy (UBM) layer formed over said metallization structure; and

a conductive bump formed directly over said UBM layer and directly over the metallization structure[[;]],

wherein [[the]]a largest linear dimension of said UBM layer is ~~larger~~greater than [[the]] a diameter of said conductive bump.

2. (Currently amended) The semiconductor device as in claim 1 wherein said metallization structure ~~further~~ comprises a top metallization layer, ~~having~~ said UBM layer is formed over the top metallization layer, and ~~thereover, wherein the~~ a thickness ~~dimensions~~ of said top metallization layer is substantially smaller than a thickness of said UBM layer.

3. (Currently amended) The semiconductor substrate as in claim 2 wherein said top metallization layer ~~includes~~comprises aluminum.

4. (Currently amended) The semiconductor device as in claim 1 wherein said UBM layer comprises (i) a bottom layer comprising[[of]] a metal, said bottom layer [[that]] adher[[es]]ing to said metallization structure, (ii) a middle layer comprising[[of]] a barrier metal, and (iii) a top layer [[of]]comprising a conductive solderable metal.

5. (Currently amended) The semiconductor device as in claim 4 wherein said bottom layer metal ~~includes~~ comprises at least one of aluminum, titanium, [[or]]and chromium.

6. (Currently amended) The semiconductor device as in claim 4 wherein said ~~middle layer includes~~ barrier metal comprises nickel.

7. (Currently amended) The semiconductor device as in claim 4 wherein said ~~middle layer includes~~barrier metal comprises vanadium.

8. (Currently amended) The semiconductor device as in claim 4 wherein said ~~top layer include~~solderable conductive material comprises copper.

9. (Currently amended) The semiconductor device as in claim 4 wherein said ~~top layer includes~~solderable conductive material comprises gold.

10. (Currently amended) A semiconductor [[chip]]device having low metallization series resistance, the semiconductor device comprising:

~~a semiconductor substrate;~~

a top metallization layer formed on [[said]]a semiconductor substrate;

a UBM layer formed over said top metallization layer; ~~wherein the thickness of said top metallization layer is substantially smaller than said UBM layer;~~ the UBM layer comprising (i) a bottom layer comprising at least one of aluminum and chromium, said bottom layer adhering to said metallization structure, (ii) a middle layer comprising vanadium, and (iii) a top layer comprising a conductive solderable metal; and

a conductive bump formed over said UBM layer[[;]]

wherein ~~the~~ a thickness of said top metallization layer is substantially smaller than a thickness of said UBM layer, and a largest linear dimension of said UBM layer is ~~larger~~greater than [[the]]a diameter of said conductive bump.

11. (Currently amended) The semiconductor ~~substrate~~device as in claim 10 wherein said top metallization layer ~~includes~~comprises aluminum.

12.–14. (Cancelled)

15. (Currently amended) The semiconductor device as in claim [[13]]11 wherein said ~~middle layer includes~~ barrier metal comprises nickel.

16. (Cancelled)

17. (Currently amended) The semiconductor device as in claim [[13]]11 wherein said ~~top layer includes~~ conductive solderable metal comprises copper.

18. (Currently amended) The semiconductor device as in claim [[13]]11 wherein said ~~top layer includes~~ conductive solderable metal comprises gold.

19. (New) The semiconductor device as in claim 1 wherein the UBM layer consists essentially of a single layer.